Si9200EY

CAN Bus Driver and Receiver

Features

- Survives Ground Shorts and Transients on Multiplexed Bus in Automotive and Industrial Applications
- Single Power Supply
- Compatible with Intel 82526 CAN Controller
- Direct Interface − No External Components Required
- Automotive Temperature Range (−40 to 125°C)

Description

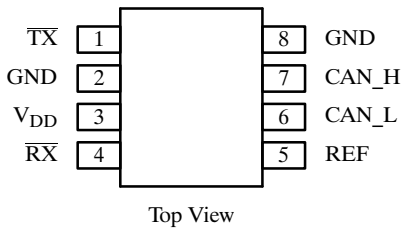
The Si9200EY is designed to interface between the Intel 82526 CAN Controller and the physical bus to provide drive capability to the bus and differential receive capability to the controller. It is designed to absorb typical electrical transients on the bus which may occur in an automotive or industrial application, and protect itself against any abnormal bus conditions. The transmitter will be disabled during these conditions and will be re-enabled when the abnormal condition is cleared.

The Si9200EY is built using the Siliconix BiC/DMOS process. This process supports CMOS, DMOS, and isolated bipolar transistors and uses an epitaxial layer to prevent latchup. The bus line pins are diode protected and can be driven beyond the V_{DD} to ground range.

The Si9200EY is offered in the space efficient 8-pin high-density surface mount plastic package and is specified over the automotive temperature range (−40 to 125°C).

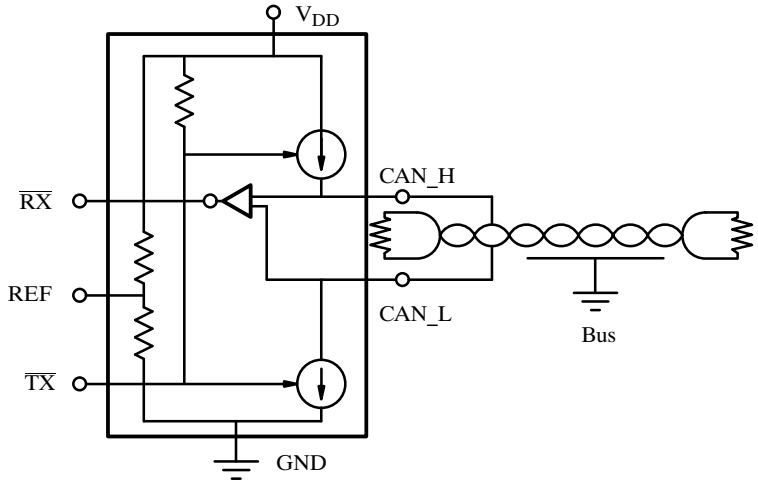
Pin Configuration and Functional Block Diagram

SO-8



Top View

Order Number:
Si9200EY



Absolute Maximum Ratings[a]

Operating Temperature (T_A) . . . . . −40 to 125°C
Junction and Storage Temperature . . . . . -55 to 150°C
Voltage On Any Pin (Except CAN_H and CAN_L)
with Respect to Ground . . . . . −0.3 to V_{DD} +0.3 V
Voltage On CAN_H and CAN_L
with Respect to Ground . . . . . −3 to +16 V
Supply Voltage, V_{DD} . . . . . −0.3 to 12 V
Continuous Output Current . . . . . ±100 mA

Thermal Ratings[b]: $R_{\Theta JA}$ . . . . . 62.5°C/W (no airflow)

Notes
a. Extended exposure to the absolute maximum ratings or stresses beyond these ratings may affect device reliability or may cause permanent damage to the device. Functional operation at conditions other than the recommended operating conditions is not implied.
b. Mounted on 1-IN^2, FR4 PC Board.

Recommended Operating Conditions

V_{DD} . . . . . 4.75 to 5.25 V
Bus Load Resistance . . . . . 60 Ω

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} = 4.75 to 5.25 V		Limits T_A = −40 to 125°C Min[b]	Typ[a]	Max[b]	Unit
Input							
$\overline{TX}$ Input Voltage High	V_{INH}			4			V
$\overline{TX}$ Input Voltage Low	V_{INL}					1	
$\overline{TX}$ Input Current Low	I_{IL}	$\overline{TX}$ = 0 V		−50		−2.0	µA
$\overline{TX}$ Input Current High	I_{IH}	$\overline{TX}$ = V_{DD}		−1.0		1.0	
Output							
Bus Recessive	V_{CAN_HR}, V_{CAN_LR}	$\overline{TX}$ = V_{INH}, R_L = ∞		2	2.5	3	V
	V_{DIF} = V_{CAN_HR} − V_{CAN_LR}			−0.5	0	0.05	
Bus Dominant	V_{CAN_HD}	$\overline{TX}$ = V_{INL}, R_L = 60 Ω		2.75	3.5	4.5	
	V_{CAN_LD}			0.5	1.5	2.25	
	V_{DIF} = V_{CAN_HD} − V_{CAN_LD}			1.5	2	3	
Reference Output	V_{REF}	−25 µA ≤ I_{REF} ≤ 25 µA		0.5 V_{DD} −0.2	0.5 V_{DD}	0.5 V_{DD} +0.2	
Receive Output (Bus Recessive Conditions)	$V_{\overline{RXH}}$	$\overline{TX}$ = V_{INH} −2.0 V ≤ V_{CAN_H}, V_{CAN_L} ≤ 7 V −1 V ≤ V_{CAN_H} − V_{CAN_L} ≤ 0.5 V (Bus Recessive)	I_{OUT} = −10 µA	V_{DD} −0.3	V_{DD} −0.05		
			I_{OUT} = −100 µA	V_{DD} −1	V_{DD} −0.2		
			I_{OUT} = −2 mA	V_{DD} −1.75	V_{DD} −1		
Receive Output (Bus Dominant Conditions)	$V_{\overline{RXL}}$	$\overline{TX}$ = V_{INH} −0.8 V ≤ V_{CAN_H} ≤ 7 V −2 V ≤ V_{CAN_L} ≤ 5.8 V 0.9 V ≤ V_{CAN_H} − V_{CAN_L} ≤ 5 V (Bus Dominant)	I_{OUT} = 10 µA		0.05	0.3	
			I_{OUT} = 100 µA		0.2	1	
			I_{OUT} = 2 mA		1	1.75	

Specifications

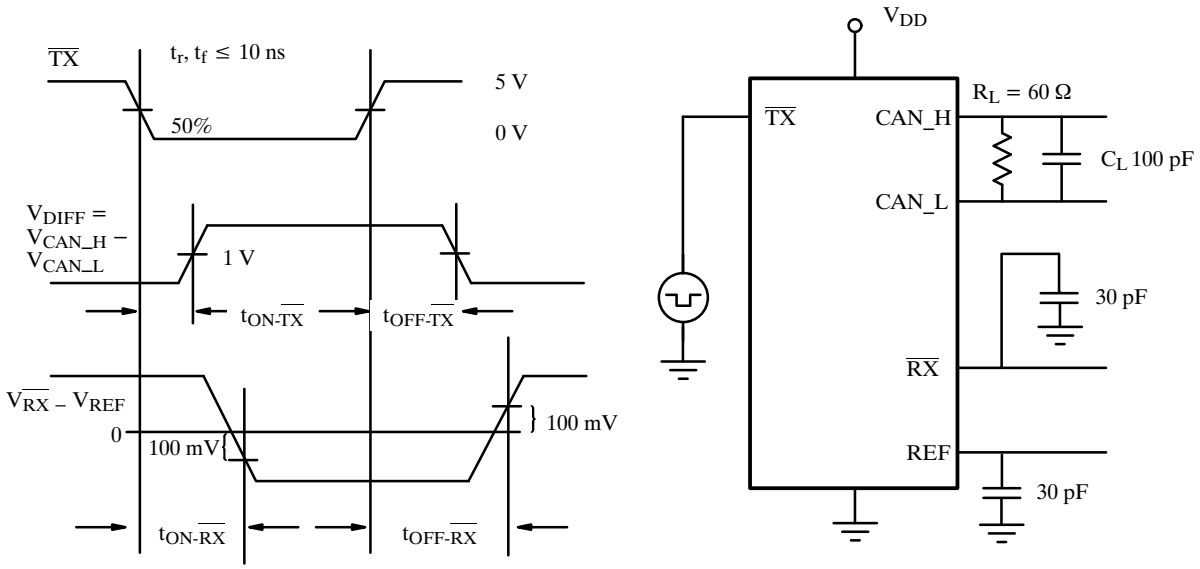
Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} = 4.75 to 5.25 V	Limits T_A = −40 to 125°C Min[b]	Typ[a]	Max[b]	Unit
Output (Cont'd)						
Internal Resistance from Bus Pins	R_{IN}, BUS_L	$\overline{TX}$ = V_{INH} (Recessive)	5		50	kΩ
	R_{IN}, BUS_H		5		50	
	R_{DIFF}		10		100	
Internal Capacitance from Bus Pins[c]	C_{IN} (CAN_H, CAN_L)				50	pF
Dynamic						
Propagation Delay − $\overline{TX}$ to V_{DIFF} High	$t_{ON-\overline{TX}}$				50	ns
Propagation Delay − $\overline{TX}$ to V_{DIFF} Low	$t_{OFF-\overline{TX}}$				50	
Propagation Delay − $\overline{TX}$ to Receive Low	$t_{ON-\overline{RX}}$				120	
Propagation Delay − $\overline{TX}$ to Receive High	$t_{OFF-\overline{RX}}$				120	
Supply						
Supply Current	I_{DD}	$\overline{TX}$ = V_{INH}, V_{DD} = 5.25 V, R_L= 60 Ω (Recessive)			25	mA
		$\overline{TX}$ = V_{INL}, V_{DD} = 5.25 V, R_L= 60 Ω (Dominant)	40		75	
Transient[c]						
Electrostatic Discharge Human Body Model	V_{ESD}	C_L = 100 pF, R_L = 1500 Ω MIL-STD-883D, Method 3015		2000		V
Bus Transient Voltage	V_{TRANS}	R_S = 1000 Ω, 1 msec	−60		60	
Protection						
Thermal Trip Point[c]	T_{TRP}		150	165	180	°C
Thermal Hysteresis[c]	T_{HYS}		10	20	30	

Notes
a. Typical values are for DESIGN AID ONLY at T_A = 25°C, not guaranteed nor subject to production testing.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
c. Guaranteed by design, not subject to production test.

Truth Table

$\overline{TX}$	Mode	Bus State	CAN_H	CAN_L	$\overline{RX}$
Low	Transmit	Dominant	High	Low	Low
High (or Floating)	Transmit and Receive	Recessive	Floating	Floating	High
High (or Floating)	Receive	Recessive	High	Low	Low

Switching Time Test Circuit



Circuit Schematic